CLAIMS

1. A circuit for detection of internal microprocessor watchdog device execution comprising a microprocessor with the internal watchdog device and with an input/output line transmitting information about microprocessor reset, and a device for resetting the microprocessor system, characterized in that, to the input/output line (11) transmitting information about the microprocessor (6) reset, a clock input CK is connected, which triggers the flip-flop (12), whose data input D and an inverted reset input /R are connected to the output of the device (19) for resetting the microprocessor system, and the inverted flip-flop (12) output /Q is connected to the input of the device (19) for resetting the microprocessor system.

2. The circuit according to claim 1, characterized in that the input/output line (11) transmitting information about microprocessor (6) reset is connected to the power supply voltage (V_{CC}) through an external resistor (10).

3. The circuit according to claim 1, characterized in that the reset of the microprocessor system resulting from the reset of the microprocessor (6) is performed when the inverted reset input /R and the flip-flop (12) data input D are in a high state and the clock input CK changes from a low to a high state.

4. The circuit according to claim 1, characterized in that the reset of the microprocessor system resulting from the reset of the microprocessor (6) is blocked by a low state of the flip-flop (12) inverted reset input /R.

5. A method for reset of a microprocessor system comprising a circuit for detection of internal microprocessor watchdog device execution, characterized in that, after disruption of microprocessor operation (6), an input/output line (11) of the microprocessor is set to a high impedance state and a system reset signal, generated by a flip-flop (12), is sent to a device for resetting the

microprocessor system, and after finishing the resetting of the microprocessor system, the input/output line (11) is set to a low state.

6. The method according to claim 5, characterized in that the microprocessor system is reset, when the flip-flop (12) has an inverted reset input /R, a data input D and a clock input CK, and the inverted reset input /R and the data input D are in a high state and the clock input CK changes from a low to a high state.

7. The method according to claim 5, characterized in that the reset of the microprocessor system resulting from the reset of the microprocessor (6) is blocked by imposing a low state on the flip-flop (12) inverted reset input /R.